Exhibit 57

UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

ACQIS, LLC, Plaintiff, v. EMC CORPORATION, Defendant.	C.A. No. 1:14-cv-13560-ADB (Leave to file granted 3/23/2017)

PLAINTIFF ACQIS, LLC'S SUR-REPLY CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

EMC's construction of "PCI bus transaction" is incorrect because it requires a physical, parallel PCI bus be "involved somewhere." (EMC's Reply at 7.) None of the asserted claims require that a physical, parallel PCI bus be involved in the claimed "PCI bus transaction." Any construction of "PCI bus transaction" that mandates the presence of a physical, parallel PCI bus is contrary to the claims, the specification, and Judge Davis's construction and must be rejected.

Moreover, EMC takes inconsistent and mutually exclusive positions with respect to "PCI bus transaction" and "encoded." In its Reply, EMC promises that its new construction of PCI bus transaction "was crafted with the express goal of capturing every disclosure in the patents, *including specifically* the Figure 8 embodiment," and "does not require an 'originating PCI bus.'" (Reply at 7 (emphasis in original).) Although EMC concedes reading the claims to require an "originating PCI bus" is incorrect, EMC's construction for "encoded"—a term that modifies PCI bus transaction in all but one of the asserted claims—requires "a PCI bus transaction that has been serialized from its ***original parallel format***." EMC cannot have it both ways.

Turning to EMC's disavowal arguments, EMC's Reply dismisses, without explanation, Acqis's and Dr. Lindenstruth's statements to the PTAB showing that Acqis did not limit "PCI bus transaction" to require "involving a PCI bus" or parallel-to-serial conversion. In light of these statements, there is no disavowal. The PTAB's Final Written Decisions further undermine EMC's position. The highly specialized PTAB relied on Dr. Lindenstruth's testimony, which is now part of the intrinsic record. The prior art references EMC raised at the PTAB both disclose transactions that *involve* a PCI bus. Acqis's PTAB win did not hinge on the lack of a physical, parallel PCI bus; rather, the PTAB found that the information content of a PCI bus transaction was never transmitted over serial links.

Next, EMC's claim that the PTAB did not construe "encoded," in an effort to discredit Acqis, mischaracterizes the PTAB record. EMC's effort to discredit Acqis lacks merit. EMC cannot credibly argue that the PTAB did not assign meaning to the term "encoded" when its appeal from the IPRs claims error with the PTAB's construction of "encoded serial bit stream of [PCI] bus transaction." The PTAB's application of "encoded" did not require parallel-to-serial conversion, and is consistent with Judge Davis's construction and Acqis's proposed construction.

Finally, EMC's suggestion that Acqis's submission of Dr. Lindenstruth's Declaration is somehow improper is incorrect as a matter of law. The Supreme Court and the Federal Circuit have consistently recognized that expert testimony is properly considered during claim construction, and reliance on such evidence is given deference on appellate review. Dr. Lindenstruth's conclusions are consistent with the intrinsic record (including his own testimony before the PTAB), and probative of how a person of ordinary skill would understand the disputed terms in the context of the patents.

This case also presents an additional reason to consider Dr. Lindenstruth's testimony because EMC argues that Dr. Lindenstruth's statements to the PTAB support EMC's constructions. The Lindenstruth Declaration responds to EMC's disavowal arguments and should be considered in the claim construction analysis.

II. EMC'S CONSTRUCTION OF "PCI BUS TRANSACTION" IS CONTRADICTED BY THE INTRINSIC RECORD AND EMC'S OWN CONSTRUCTION OF "ENCODED"

EMC's construction of "PCI bus transaction," which "requires only that there is a PCI bus involved ***somewhere***," is incorrect because it is contradicted by the intrinsic record. The asserted claims do not require that a physical, parallel PCI bus receive the transactions or be

"involved somewhere." (*See, e.g.*, EMC Br., Appx. B at 3; Ex. A[1] at ¶ 119; Lindenstruth Decl. at ¶¶ 114-115[2]; *see also id.* at ¶¶ 98-116.) Moreover, the claims specifically describe the physical layer that the PCI bus transactions are sent over, i.e., serial low-voltage differential signal channels—not a parallel PCI bus. (*See, e.g.*, Ex. D at claim 54; Ex V at claim 31; Lindenstruth Decl. at ¶¶ 101-104.)

Next, EMC's position that the claims ***do not require*** an "originating PCI bus" contradicts its construction of encoding which ***does require*** an originating parallel PCI bus. "Encoded" modifies "PCI bus transaction" in all but one of the asserted claims. (EMC Br., Appx. B at 1-2.) EMC concedes what Acqis has argued all along—requiring an originating PCI bus reads out the embodiments disclosed in Figure 8 of the '873 patent.[3] (Reply at 6-7.) EMC's position with respect to "PCI bus transaction" requires rejecting EMC's construction of "encoded."

Finally, EMC's claim scope disavowal argument is meritless. Acqis did not argue that a PCI bus was required by the asserted claims. (Acqis Br. at 11-12; Ex. P at 46:11-22, 47:9-48:12; Ex. A at ¶ 119; Ex. B at ¶ 114; Lindenstruth Decl. at ¶¶ 137-145.)

A. The Claims Do Not Require "involving" A PCI Bus

Claim construction starts with the claims. *Phillips v. AWH*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*) ("It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude.") (quotations and citations omitted). As explained in Acqis's Brief, the claims and specifications of the asserted patents

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[1] The cited exhibits are attached to the Declaration of James P. Brogan submitted with Acqis's Claim Construction Brief, unless otherwise noted. (D.I. 189-3.)

[2] The Lindenstruth Declaration refers to the Declaration of Prof. Dr. Volker Lindenstruth submitted with Acqis's Claim Construction Brief, unless otherwise noted. (D.I. 189-2.)

[3] *See also* Ex. Y ('119 Patent) at Fig. 15; Ex. V ('814 Patent) at Fig. 18; Ex. W ('984 Patent) at Fig. 18; Ex. X ('171 Patent) at Fig. 15; Ex. M ('468 Patent) at Fig. 18; '416 Patent at Fig. 8; '487 Patent at Fig. 8; '624 Patent at Fig. 8; Lindenstruth Decl. at ¶¶ 107-111. The embodiments disclosed in Figures 20 of the '468 (Ex. M) and '984 (Ex. W) Patents also foreclose the use of an "originating PCI bus." (Lindenstruth Decl. at ¶¶ 112-113.)

require a construction of "PCI bus transaction" that is not limited to a particular physical layer, i.e. a physical, parallel PCI bus. (Acqis Br. at 6-12, 15-18.) The claims define the physical layer as a serial low-voltage differential signal channel, and not a parallel PCI bus. This construction—which Acqis has consistently maintained—was confirmed by Judge Davis: "Defendants have failed to show that a PCI bus transaction necessarily implies the presence of a PCI bus." (Ex. U at 10.) EMC does not point to one claim that requires the presence of a physical, parallel PCI bus. This is because EMC developed its construction of "PCI bus transaction" to create a non-infringement defense; it is not grounded in the claims.

EMC does not dispute that Figure 8 of the '873 Patent discloses PCI bus transactions that are created and transmitted serially without an originating physical, parallel PCI bus. (Reply at 6-7.) EMC concedes, agreeing with Judge Davis, that there is no physical, parallel PCI bus disclosed on the computer module in the embodiment described in Figure 8 of the '873 Patent (and similar embodiments throughout the asserted patents) and that no PCI bus is required to create the claimed encoded serial PCI bus transaction. (*Id.*)

EMC now argues, after modifying the construction it proposed to Judge Davis, that a physical, parallel PCI bus need only be "involved somewhere," in the console, for example. (Reply at 7.) However, EMC's proposed construction is incorrect. The claimed "PCI bus transaction" is never required to involve a physical, parallel PCI bus. Claim 24 of the '171 Patent is exemplary (Ex. X (emphasis added).):

> providing a computer module, the module comprising
> a processor unit,
> a connection program,
> an integrated interface controller and bridge unit ***to output an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction***, the integrated interface controller and bridge unit coupled to the central processing unit ***without any intervening PCI bus***…

As shown above, ***without an intervening PCI bus***, the "encoded serial bit stream address and data bits of ***[PCI] bus transaction***" is ***output*** form the integrated interface controller and bridge unit. There is no requirement in the claim that (1) the claim originates on a physical, parallel PCI bus, or (2) ends up on a physical, parallel PCI bus. Rather, claim 24 recites, in plain and explicit terms, a PCI bus transaction without a physical, parallel PCI bus.

The asserted claims also never require a physical, parallel PCI bus in the console. Take claim 48 of the '984 Patent, for example (Ex. W (boxes added to show console related limitations and italics show the PCI bus transaction limitation).)

> 48. A computer system comprising:
>
> a console comprising a power supply; and
>
> a computer module coupled to the console, the computer module comprising
>
> a central processor unit,
>
> a connection program,
>
> a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,
>
> an integrated interface controller and bridge unit coupled to the low voltage differential signal channel ***to communicate an encoded serial bit stream of address and data of [PCI] bus transaction***, the integrated interface controller and bridge unit directly coupled to the central processing unit ***without any intervening PCI bus***, and
>
> a mass storage device coupled to the central processing unit,
>
> wherein the computer module is configured to receive power from the power supply, and the computer module is configures to communicate, through Ethernet, to a local area network upon coupling of the computer module to the console.

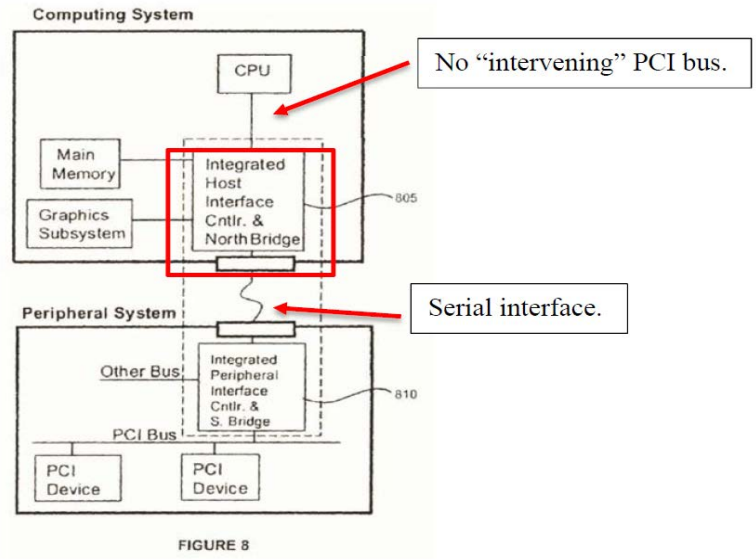
(*See, also*, Ex. X at cl. 24.) Even when a claim recites a "PCI bus transaction" in the console, the physical layer is limited, just as it is in the computer module, to "a first low voltage differential signal (LVDS) channel comprising two unidirectional serial channels"—not a physical, parallel PCI bus. (Ex. V at cl. 24.)

B. EMC Concedes That Its Construction Of "encoded" Reads Out the Embodiments Disclosed In Figure 8

EMC accuses Acqis of "adding new requirements to its constructions that EMC does not propose or intend." (Reply at 1.) However, while EMC's construction of "PCI bus transaction" may not require an *originating* PCI bus, EMC's construction of "encoded" *requires an originating parallel PCI bus*. (EMC Br. at 15 (EMC proposes that "encoded" mean "a PCI bus transaction that has been serialized ***from its original parallel format***.") (emphasis added).) By attempting to construe "encoded" to require a PCI bus transaction in its original parallel format, EMC requires that the claimed "encoded … PCI bus transaction" originate on a physical, parallel PCI bus. (EMC Br., Appx. B at 1-2.) EMC's argument in support of "PCI bus transaction" cannot be squared with its construction of "encoded."

The "encoded … PCI bus transaction" in many of the claims originates from the Computing System side of the embodiment shown in Figure 8 below (disclosed in nine out of eleven asserted patents)[4] (annotations added).

[4] *See also* Ex. Y ('119 Patent) at Fig. 15; Ex. V ('814 Patent) at Fig. 18; Ex. W ('984 Patent) at Fig. 18; Ex. X ('171 Patent) at Fig. 15; Ex. M ('468 Patent) at Fig. 18; '416 Patent at Fig. 8; '487 Patent at Fig. 8; '624 Patent at Fig. 8; Lindenstruth Decl. at ¶¶ 107-111. The embodiments disclosed in Figures 20 of the '468 (Ex. M) and '984 (Ex. W) Patents also foreclose the use of an "originating PCI bus." (Lindenstruth Decl. at ¶¶ 112-113.)



If EMC's constructions for "PCI bus transaction" and "encoded" were adopted, exemplary claim 24 of the '171 Patent (which covers Figure 8) would read as follows: "a computer module, the computer module comprising … an integrated interface controller and bridge unit to output [**a transaction, defined by the industry standard PCI Local Bus Specification, involving a PCI bus, that has been serialized from its original parallel format]**, the integrated interface controller and bridge unit coupled to the central processing unit ***without any intervening PCI bus***." (Ex. X at cl. 24; EMC Br. at 9, 15, Appx. B at 1.) EMC's construction of "encoded" directly contradicts EMC's admission (and the claims' requirement) that "no originating PCI bus" is found in Figure 8 and the claims that cover it. (Reply at 6-7.) Requiring an originating PCI bus to create an "encoded … PCI bus transaction" reads out the embodiments disclosed in Figure 8 and the claims that cover those embodiments.[5]

[5] *See, e.g.*, Ex. W ('984 Patent) at claim 48 (including the limitation "the integrated interface controller and bridge unit directly coupled to the processor without any intervening PCI bus."); Ex. X ('171 Patent) at claim 24 (including the limitation "the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus."); Ex. Y ('119 Patent) at claim 38 (including the limitation "a peripheral bridge directly coupled to said microprocessor unit without any intervening PCI bus."); Ex. D at claim 54 ('873 Patent) (including

C. Acqis's Arguments To The PTAB Did Not Require A "PCI bus transaction" To "involve a PCI bus"

The sole issue in dispute before the PTAB was whether the Horst reference disclosed communicating an encoded PCI bus transaction over a serial channel. (Ex. Q at 14-15; Ex. R at 14-15; Lindenstruth Decl. at ¶¶ 146-153.) Acqis overcame the prior art by arguing, in part, that the Horst reference did not disclose communicating encoded PCI bus transactions over a serial channel even where the PCI bus transaction was received from a *parallel PCI bus*. (Ex. Q at 15 n.4 ("Horst teaches that the TNet bus interface translates an I/O bus transaction, such as a PCI bus transaction, into a TNet transaction *before* the transaction is encoded for serial communication…."); Ex. R at 15 (same); Lindenstruth Decl. at ¶¶ 137-153.) The Horst system and its physical, parallel PCI bus is shown below. (Ex. Q at 8; Ex. R at 9 (annotations added).)

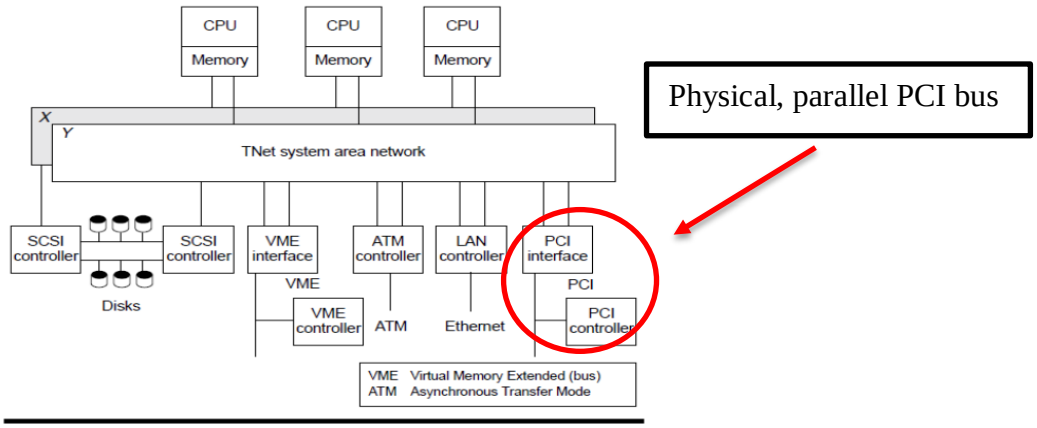


Figure 2. CPU cluster connected with the TNet system area network.

EMC mischaracterizes the record; it was undisputed that the prior art before the PTAB included a physical, parallel PCI bus. (Reply at 8; Lindenstruth Decl. at ¶¶ 151-153.)

The PTAB record is clear. Acqis never argued that the claims *require* a physical, parallel PCI bus, only that the presence of a PCI bus was an indicator that a PCI bus transaction occurred.

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the limitation "a peripheral bridge directly coupled to the processor."); Ex. M ('468 Patent) at claim 37 ("a central processing unit directly connected to a first [LVDS] channel to convey a first encoded serial bit stream of address and data bits of a [PCI] bus transaction.").

(Acqis Br. at 11-12; Ex. P at 46:11-21, 47:19-48:2.) Dr. Lindenstruth, whose testimony during the PTAB proceedings became part of the prosecution history and therefore part of the intrinsic record, also made clear that "PCI bus transaction" did not require a physical, parallel PCI bus. (Ex. A at ¶ 119 ("I note that a PCI bus is parallel and the claims discuss communicating PCI bus transactions serially, so the *claims do not require that the PCI bus transaction occur on a PCI bus*; they require the address and data phases of a PCI bus transaction.") (emphasis added); Ex. B at ¶ 114 (same); Lindenstruth Decl. at ¶¶ 137-145.)

EMC's claim that the PTAB construed "PCI bus transaction" to require a PCI bus is also wrong. The PTAB construed "PCI bus transaction" to mean "PCI industry standard bus transaction." (Ex. Q at 6-7; Ex. R at 6-7.) There is no physical bus requirement, and as applied, the PTAB's construction of "PCI bus transaction" refers to information, not to the physical layer. (*See, e.g.*, Ex. Q at 15 (explaining that a PCI industry standard bus transaction could travel over a set of serial TNet links).) The PTAB understood that a PCI bus transaction could travel over a serial channel. (Lindenstruth Decl. at ¶¶ 98-100.) EMC's disavowal arguments rely on misleading and incomplete citations to the record, and should be rejected.

III. THE PTAB ASSIGNED MEANING TO "ENCODED" AND EMC CONCEDES THAT PARALLEL-TO-SERIAL CONVERSION IS NOT REQUIRED FOR EMBODIMENTS DISCLOSED IN THE ASSERTED PATENTS

As discussed in Section II(B) above, EMC concedes that its construction of "encoded" would exclude the embodiment disclosed in Figure 8 of the asserted patents. EMC's construction of "encoded" should be rejected for that reason alone.

A. The PTAB Assigned Meaning To The "encoded" Terms

Instead of attempting to explain how its contradictory positions can coexist, EMC attempts to play "got you" by accusing Acqis of falsely claiming that the PTAB construed "encoded." (Reply at 10.) However, in reaching its conclusion that the challenged claims are not

invalid, the PTAB necessarily applied a construction to the term "encoding…PCI bus transaction." In fact, EMC's primary argument on appeal from its PTAB loss is that the Board erred in its ***implied construction*** of "encoded serial bit stream of [PCI] bus transaction." (Ex. FF at 2 ("The Board, without support in the claims or specification, read a negative no-translation limitation into the claim phrases 'encoded serial bit stream of [PCI] bus transaction'…."); Ex. EE-1 at 3.)

In the IPRs, and consistent with Judge Davis's construction and the testimony of Dr. Lindenstruth, the Board recognized that encoding is not tied to the origin of the information. (Ex. U at 11; Ex. A at ¶ 121-125; Lindenstruth Decl. at ¶¶ 117-126, 146-153.) For example, the Board considered 8B/9B encoding as meeting the encoding limitation. (Ex. Q at 15 n.4. (recognizing that Horst taught 8B/9B encoding and that "the TNet bus interface outputs a TNet transaction that has been encoded, not a PCI industry standard bus transaction that has been encoded.").) 8B/9B encoding does not require parallel-to-serial conversion. (Ex. A at ¶ 115 ("8b/9b is a serial line code that uses a simple, reversible algorithm to represent 8-bit words in 9 characters…."); Ex. B at ¶ 105 (same).) The Board implicitly assigned meaning to the term "encoded" and it did not require parallel-to-serial conversion. (Lindenstruth Decl. at ¶¶ 151-153.)

B. EMC Concedes That Parallel-to-Serial Conversion Is Not Required To Create An "encoded … PCI bus transaction"

In addition to the fact that Judge Davis and the PTAB never construed "encoded" to require parallel-to-serial conversion, EMC now concedes that the embodiment disclosed in Figure 8 does not include a physical, parallel PCI bus on the computer module. (Reply at 6-7 (showing figure with "No originating PCI bus" on the computer module).) Taking EMC at its word, claims that cover the embodiment of Figure 8 (and similar embodiments described throughout the asserted patents) must create an "encoded serial bit stream of address and data

bits of [PCI] bus transaction" without an originating physical, parallel PCI bus. EMC's construction of "encoded" should be rejected because it requires an "original parallel format." (Reply at 6; § II(B) above; *see also* Acqis Br. at 5; Lindenstruth Decl. at ¶¶ 60, 144, 107-116.)

IV. DR. LINDENSTRUTH'S TESTIMONY IS RELEVANT TO CLAIM CONSTRUCTION

Dr. Lindenstruth's Declaration is proper evidence of how a person of ordinary skill in the art would understand the disputed claims. *Phillips*, 415 F.3d at 1318; (Lindenstruth Decl. at ¶¶ 90-96 (explaining that Dr. Lindenstruth is a person of ordinary skill in the art, or "POSA").) Dr. Lindenstruth's Declaration is also directly responsive to EMC's disavowal argument—based in part on Dr. Lindenstruth's testimony before the PTAB. (Lindenstruth Decl. at ¶¶ 134-153; EMC Br. at 19, 24.) Dr. Lindenstruth's testimony in the IPRs, credited by the PTAB and part of the intrinsic record, shows that the claims do not require a physical, parallel PCI bus or parallel-to-serial conversion. (Ex. Q at 11, 13, 15 n.4 (citing Lindenstruth Decl. (Ex. 2021) throughout); Lindenstruth Decl. at ¶¶ 134-153.) Dr. Lindenstruth's opinions are highly relevant to this dispute and should be considered as part of the claim construction analysis.

A. The Court Can, and Should, Consider Dr. Lindenstruth's Testimony

Broad consideration of expert testimony is consistent with the canons of claim construction; after all, "[i]t is the person of ordinary skill in the field of the invention through whose eyes the claims are constructed." *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998); *see also Phillips*, 415 F.3d at 1318 ("[E]xtrinsic evidence in the form of expert testimony can be useful to a court for a variety of purposes, such as … to ensure the court's understanding of the technical aspects of the patent is consistent with that of a person of ordinary skill in the art…."); *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 838 (2015) (noting claim construction has "evidentiary underpinnings" and district courts may have to make "credibility judgments" about witnesses to construe claims properly).

Dr. Lindenstruth co-authored one of EMC's primary prior art references and submitted sworn testimony in the IPRs that is part of the intrinsic record. Dr. Lindenstruth's testimony will assist the Court with understanding how a POSA would understand the claim terms. (Lindenstruth Decl. at ¶¶ 90-97.) Dr. Lindenstruth is also uniquely capable of rebutting EMC's disavowal arguments based on his personal knowledge of the record and involvement in the IPRs. In this case, Dr. Lindenstruth testified that:

- "PCI bus transaction" used in the patent claims refers to the information sent over the claimed serial channel, and not to the type of physical bus (the wires) over which the information travels. I disagree with EMC's construction because it adds the limitation of a parallel PCI bus; a POSA would also disagree. (Lindenstruth Decl. at ¶¶ 15, 98-116.)

- [EMC's] construction [of "encoded"] is incorrect because, like PCI bus transaction, it requires a physical parallel PCI bus and an "original parallel format." I also disagree with EMC's proposed construction because it limits the term "encode" to require parallel-to-serial conversion. (*Id.* at ¶¶ 19, 117-126.)

- During the IPR proceedings, I did not testify that the challenged claims required a parallel PCI bus or parallel-to-serial conversion. (*Id.* at ¶¶ 22, 137-145.)

- Based on my review of the Final Written Decisions issued by the PTAB, a POSA would understand that the PTAB did not distinguish the claims of the Acqis patents from the prior art because the prior art lacked either a parallel PCI bus or parallel-to-serial conversion of a PCI bus transaction as EMC claims. (*Id.* at ¶¶ 24, 146-153.)

- [T]he PTAB distinguished the prior art from the claims of Acqis's patents because the prior art did not communicate an encoded PCI industry standard bus transaction in serial form." (*Id.* at ¶¶ 25, 151-153.)

Dr. Lindenstruth's opinions are grounded in the language of the claims and the specifications, to which his Declaration cites extensively. (*See, e.g.*, *id.* at ¶¶ 98-133 (providing analysis for constructions of the disputed terms), ¶¶ 134-153 (providing analysis with respect to positions taken before the PTAB).) EMC does not cite any examples where Dr. Lindenstruth's

testimony contradicts the intrinsic record. Dr. Lindenstruth's testimony should be considered in the claim construction analysis.

B. Dr. Lindenstruth's Testimony Before the PTAB Is Part of the Intrinsic Record and Must Be Considered As Part of the Claim Construction Analysis

Dr. Lindenstruth's testimony before the PTAB supports adopting Acqis's proposed constructions and rejecting EMC's. With respect to "PCI bus transaction," Dr. Lindenstruth testified, "I note that a PCI bus is parallel and the claims discuss communicating PCI bus transactions serially, so the claims do not require that the PCI bus transaction occur on a PCI bus." (Ex. Q at ¶ 119; Ex. R. at ¶ 114.) As to "encoded," Dr. Lindenstruth testified that "encode" means "a reversible operation that turns a signals into bits, packetizes bits into a specified size packet, or orders bits onto one or more serial transmission lines." (Ex. A at ¶ 125; Ex. B at ¶ 120.) Dr. Lindenstruth identified two types of encoding in the asserted patent specifications that do not require parallel-to-serial conversion, (1) packetizing bits into a specified size packet, or (2) ordering bits onto one or more serial transmission lines. (Ex. A at ¶¶ 122-124; Ex. B at ¶¶ 116-119; Lindenstruth Decl. at ¶¶ 117-125.) The PTAB found Dr. Lindenstruth's testimony to be credible and it supports Acqis's claim constructions in this case. (Ex. Q at 11, 13, 15 n.4 (citing Lindenstruth Decl. (Ex. 2021).) EMC's proposed constructions and claim scope disavowal arguments are without merit.

V. "COMMUNICATING … PCI BUS TRANSACTION" AND RELATED TERMS NEED NO CONSTRUCTION

The resolution of the parties' dispute over "PCI bus transaction" and "encoded" will obviate the need for construing "communicating" and related terms. (Acqis Br. at 22.) Furthermore, Dr. Lindenstruth's unrebutted testimony confirms that: (1) the intrinsic record contradicts EMC's proposed construction, (2) that a POSA would readily understand the meaning of the terms EMC seeks to construe, and (3) Acqis did not take the position that

"communicating" requires "all address, data, and control bits, without discarding any of those bits." (Lindenstruth Decl. at ¶¶ 127-133.) The Court should reject EMC's proposed construction.

VI. CONCLUSION

For the foregoing reasons, Acqis respectfully requests that this Court adopt Acqis's proposed claim constructions and reject EMC's proposed constructions.

Dated: March 23, 2017

Respectfully submitted,

/s/ James Brogan

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CERTIFICATE OF SERVICE

I hereby certify that this document filed through the CM/ECF system will be sent electronically to the registered participants as identified on the Notice of Electronic Filing (NEF) and paper copies will be sent to those indicated as non-registered participants on March 23, 2017.

/s/ James Brogan

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